Docket #: S10-279

Optoelectronic Device Integration with Waveguides

Stanford researchers have patented a fabrication process for monolithic integration of different epitaxial materials on the same substrate for improved coupling of optoelectronic devices. Monolithic integration without bonding significantly reduces packaging cost and device size. The process also solves the problem of material mixing without degrading the performance of the final device. One embodiment of the invention uses silicon dioxide (SiO_2) as the thin, insulating layer between the waveguide and optoelectronic device. SiO_2 is compatible with silicon processing and certain methods of growth for germanium and silicon-germanium alloys, which simplifies device fabrication.

Miller Lab silicon photonics technology available for licensing includes:
“Ge-Si quantum well structures” U.S. Patent No. 7,599,593.
“Integration of optoelectronics with waveguides using interposer layer” U.S. Patent 8,824,837.
“Selective area growth of germanium and silicon-germanium in silicon waveguides for on-chip optical interconnect applications." U.S. Patent No. 9,368,579.
"Self-aligned semiconductor ridges in metallic slits as a platform for planar tunable nanoscale resonant photodetectors." U.S. Patent No. 8,829,633.
"Universal Linear Components." U.S. Patent Application No. 14/092,565.
"Field-Programmable Optical Component." U.S. Patent Application No. 15/080,170.
“Phase shifting by mechanical movement “ U.S. Patent Application No. 15/380,062 (Stanford docket 15-472)

Applications

- Optoelectronic Devices such as modulators, detectors, and lasers
- Computers and other information processing systems, switching systems, data communications

Advantages

- **Economical:**
  - Monolithic integration does not require bonding which significantly reduces the packaging cost and device size.
  - SiO2 used in this example is compatible with silicon processing which simplifies device fabrication.
- **Versatile** - SiO_2 was used as interposer layer. This technique also applies to other insulating material, such as Si_3N_4, and devices fabricated of Si, Ge, SiGe, III-V alloys and II-VI alloys.

Publications

- US Patent Application 20120219250

Patents

- Published Application: 20120219250
- Issued: 8,824,837 (USA)

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