Docket #: S11-311

Heterostructure 1-Transistor DRAM with Improved Retention Time

Engineers in Prof. Krishna Saraswat's laboratory have developed a scalable 1-transistor (1T) dynamic random access memory (DRAM) with a gallium phosphide (GaP) source-drain on silicon. Because a 1T DRAM does not have a capacitor (compared to conventional 1-transistor 1-capacitor DRAM), they can achieve higher device density and are more compatible with CMOS embedded memory applications. This technology then takes advantage of GaP's high bandgap (2.26eV) to overcome retention time issues that have been problematic for traditional 1T DRAM. Finally, the device can be made in the FinFET structure, enabling better scalability than conventional planar silicon 1T DRAM. This 1T DRAM could be used for either stand-alone or embedded memory applications.

Applications

- **Memory:**
  - stand alone DRAM
  - embedded memory applications.

Advantages

- **Improved retention time** - 100-150X improvement over a similar SiSD 1T DRAM cell (10s at 25^{o}C and 1.5s at 85^{o}C)
- **Scalable** down to at least 15nm gate length without much degradation in performance
- **Feasible fabrication:**
  - compatible with MOSFET structures and technology
  - GaP is nearly lattice matched with silicon which enables easy integration and defect-free epitaxial growth on bulk silicon

- **Low thermal budget**

Publications

- Pal, A., Nainani, A., Gupta, S., Saraswat, K.C. "Performance Improvement of One-Transistor DRAM by Band Engineering," *Electron Device Letters, IEEE* (Volume:33, Issue: 1) 2013
- Pal, A., Saraswat, K.C., Nainani, A., Zhiyuan Ye, Xinyu Bao, Sanchez, E. "GaP Source-Drain Vertical Transistor on Bulk Silicon for 1-Transistor DRAM Application," 5th International Memory Workshop (IMW), 26-29 May 2013 Monterey, CA
- Pal, A., Nainani, A, Zhiyuan Ye, Xinyu Bao, Sanchez, E., Saraswat, K.C. "Electrical Characterization of GaP-Silicon Interface for Memory and Transistor Applications" *IEEE Transactions on Electron Devices* (volume: 60, Issue 7), 2013
- Pal, A., Nainani, A., Saraswat, K.C. "Addressing Key Challenges in 1T-DRAM: Retention Time, Scaling and Variability - Using a Novel Design with GaP Source-Drain" International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), 3-5 Sept. 2013, Glasgow
- TRANSISTOR-BASED APPARATUSES, SYSTEMS AND METHODS (U.S. Patent Application, Publication No. 2013-0307025)

Patents

- Published Application: 20130307025

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