Docket #: S04-132

A Method for Heteroepitaxial Growth of Germanium on Silicon

Stanford researchers have patented a growth and anneal process for growing heteroepitaxial-germanium directly onto silicon. Low surface roughness and defects are confined near the Si/Ge interface, thus not threading to the surface as expected in this lattice mismatched system. This process creates defect-free, fully-relaxed, smooth, single crystal germanium layers on silicon without a graded buffer layer or any chemical-mechanical planarization. This technology simplifies heterogeneous integration of germanium CMOS and optoelectronic devices on silicon.

Applications

- Ge MOSFETs with advanced high-K gate dielectric and metal gate integrated on Si Ge Photodetectors, Metal-Semiconductor-Metal (MSM) and p-i-n for optical interconnects
- Ge based lasers integrated on Si
- Bonding for Germanium on Insulator (GOI) fabrication and 3D applications
- GaAs growth on CVD Ge for the eventual integration of Ge
- Si and GaAs Ge/Si quantum well devices for DRAM, photonic and spintronic applications
- Ge thin film photovoltaic devices
- III-V on Si Tandem photovoltaic devices

Advantages

- Simple, in-situ hydrogen anneal
- No Chemical Mechanical Polishing (CMP) necessary
- No thick SiGe Graded layer necessary
- High purity epi-Ge achieved as compared to bulk germanium

Publications

- A. Nayfeh, C. O. Chui, T. Yonehara and K. C. Saraswat, "Fabrication of high-quality p-MOSFET in Ge grown heteroepitaxially on Si," IEEE Electron Device Lett., Vol. 26, pp. 311-313, May 2005.
- A. Nayfeh, C. O. Chui, . K. C. Saraswat and T. Yonehara, "Effects of hydrogen annealing on heteroepitaxial-Ge layers on Si: Surface roughness and electrical quality," Appl. Phys. Lett., Vol. 85, No. 14, pp. 2815-2817, 4 Oct. 2004

Patents

- Published Application: 20060019466
- Published Application: WO2006012544
- Published Application: 20090061604
- Issued: 7,495,313 (USA)
- Issued: 7,772,078 (USA)
- Issued: 7,919,381 (USA)

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