Docket #: S06-086

Heterostructure Negative Differential Resistance Device

Researchers in Prof. James Plummer's laboratory have developed a patented silicon-compatible negative differential resistance (NDR) device with high peak to valley current ratios (PVCR's). This invention is based on SiGe gated tunneling diodes and is arranged for selective passage of current through relatively high tunneling efficiency regions and relatively low tunneling efficiency regions. This design has excellent scalability since a minimum sized structure can now be inserted into a DRAM (dynamic random access memory) cell.

Applications

- **Semiconductors**
  - memory
  - microprocessors
  - ASIC

Advantages

- **Large peak currents and very high PVCR** - as high as 295 at room temperature/1113 at -65^{O}C
- **Excellent scalability** - because the peak current comes from tunneling and does not scale with channel length
- **CMOS-compatible** - the process is silicon-compatible, with no III-V materials, so it can easily be integrated into conventional CMOS technology
- **Robust and high yield process**

Publications

- Y. Liang, K. Gopalakrishnan, P.B. Griffin and J. D. Plummer, “From DRAM to SRAM with a novel sige-based negative differential resistance (NDR) device,” IEEE Electron Devices Conference, Washington DC, Dec. 2005.

Innovators

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