Docket #: S09-168

Delayed Decision Feedback Sequence Estimator

In high-speed serial links, most receivers use decision feedback equalization to deal with channel loss. While this corrects for the effect of channel dispersion, it does not take into account the dispersed energy in making the decision about each bit. To do that requires a soft-decision Viterbi decoder. Unfortunately these get very complex when the energy is spread over many samples. Since most of the energy is concentrated in a few bits, one would like to use a Viterbi decoder, combine with a DFE to cancel out the remaining bits. These systems have been proposed, but currently must be run at the bit rate, which is not possible in very high-speed links. Stanford engineers have broken through this bottleneck, and created a delayed decision feedback sequence estimator (DDFSE) that operates at a clock rate of 1/M of that of the received data and can decode the data in parallel. The key is removing errors that can be introduced by partitioning the data into chunks.

Applications

- High speed communications
- High-performance communications

Advantages

- Accelerated parallel processing
- Improved error detection

Patents

- Published Application: 20090268804

- Issued: 8,116,366 (USA)

Innovators

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