

Docket #: S13-406

Post-Silicon Validation for Complex SoCs with Accelerators

Stanford researchers have designed a systematic technique for post-silicon validation in system-on-chips (SoCs). This novel approach provides rapid speed and high error coverage validation that can precisely match the design specifications of accelerators or customized hardware (i.e. high-definition video accelerators, power management circuitry, etc.). Results demonstrate that this approach improves error detection latencies of bugs by five orders of magnitude and 12-fold fewer undetected errors. Such significant improvements enable quick bug localization and fixing, and overcome major system validation impediments.

Publications

- [*Hybrid Quick Error Detection \(H-QED\): Accelerator Validation and Debug using High-Level Synthesis Principles*](#)

Patents

- Published Application: [WO2016200718](#)
- Published Application: [20180165393](#)
- Issued: [10,546,079 \(USA\)](#)

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