Multi-bit per cell Resistance Distribution Control for Fast, Efficient Read and Program for Resistive RAM

Researchers in the Robust Systems Group at Stanford University developed a method for dividing the available resistance window in a multi-bit per cell Resistive RAM into varying resistance distributions to improve read and program performance. Controlling resistance distribution is critical for optimal read and program performance in multi-bit per cell ReRAM. Stanford researchers' method assigns nonuniform resistance ranges based on the intrinsic variation of ReRAM memory cells; and assigns non-uniform gaps between the distributions based on sense-amplifier margin requirements. This approach achieves the best read and program performance, and makes ReRAM a more competitive non-volatile memory option for wearables and Internet of Things technology.

Stage of Research

Researchers successfully tested the method at the array level on a 4Kb 1T1R HfO₂based ReRAM using 130nm silicon CMOS technology for storing 3 bits per each cell where 8 resistance distributions were precisely controlled.

Related work optimizing read and write performance for ReRAM is covered in Stanford Docket 18-124.

Applications

 Non-volatile memory – especially for cost-sensitive, low power consumption, or lower memory density applications including solid state drives, mobile computing, wearables, and other IoT technology.

Advantages

- Energy efficient
- Faster read and write performance compared to flash memory
- More stable technique to compensates for temperature-dependent shifts in the distributions that may affect the sensing margin

Publications

 Binh Q. Le, Alessandro Grossi, Elisa Vianello, Tony Wu, Giusy Lama, Edith Beigne, H.S. Philip Wong, and Subbhasish Mitra, <u>"Resistive RAM With Multiple</u> <u>Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell"</u>. *IEEE Transactions on Electron Devices*, November 26, 2018.

Patents

- Published Application: 20210035638
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