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Two-Fold Reduction of Switching Current Density in Phase-Change Memory

Researchers at Stanford have developed a low-power phase-change memory (PCM) technology with interfacial thermoelectric heating enhancement. This scalable innovation, with ~2x reduced reset power and reset current density, could be a promising route for high density data storage applications. While PCM technology has already been adopted in commercial products as a promising storage-class memory, high switching current density and switching power remain key challenges, including in emerging applications such as neuromorphic and in-memory computing. The Stanford technology leverages a substantial, positive thermoelectric coefficient in PCM materials to generate additional heating at an interface with another material, enabling memory switching with a large reduction in current and power. Interfacial thermoelectric engineering is applied to a PCM cell using a class of thermoelectric materials with negative thermoelectric coefficient (e.g., bismuth telluride, Bi2Te3) to induce efficient heating at lower power and current. Other thermoelectric materials with large negative thermoelectric coefficient (e.g., PbTe, La3Te4, InSe, Si0.8Ge0.2) could also be used instead, and these could be further optimized by changing their composition, deposition, and thickness.

Stage of Development

The researchers have demonstrated their PCM technology leverages thermoelectric heating at the PCM interface to provide a ~2x reduction in the reset current density and power at a similar voltage.

Applications

- High density data storage

Advantages

- Reduction of switching current density and switching power is a critical problem facing the industry
- Innovative yet simple and scalable
- ~2x less power and reset current density compared to control PCM devices
- Enhanced thermoelectric heating with reduced reset power

Publications

- Khan, Asir Intisar, et al. "Two-Fold Reduction of Switching Current Density in Phase Change Memory Using Bi?Te? Thermoelectric Interfacial Layer." *IEEE Electron Device Letters* 41.11 (2020): 1657-1660.

Patents

- Published Application: 20220115590

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